CBCS SCHEME

USN | | | | | | | | | | |

15NT54

Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Systems Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain and design a binary full adder with a truth table and Boolean expressions for the outputs. **(08 Marks)**

b. What are comparators? Design 1 bit binary comparator and implement with suitable logic gates. **(08 Marks)**

OR

2 a. Explain briefly about combinational circuits and sequential circuits. **(06 Marks)**

b. State and explain the applications of a multiplexer. **(04 Marks)**

c. Describe the implementation of logic for basic gates using NAND and NOR gates. **(06 Marks)**

Module-2

3 a. Write a short note on parity generators. **(08 Marks)**

b. Write a verilog code for 4-bit ripple carry adder. **(08 Marks)**

OR

4 a. Write a verilog code for 2:1 MUX using IF and CASE statement. **(08 Marks)**

b. Design a 4-bit comparator using 2 bit comparator. **(08 Marks)**

Module-3

5 a. Explain the working of D-latch using NOR gate with truth table, symbol. **(08 Marks)**

b. Write a short note on shift registers. Name the types of shift registers. **(04 Marks)**

c. Draw logic diagram and truth table for updown counter. **(04 Marks)**

OR

6 a. Explain the working of Asynchronous counter with truth table. **(10 Marks)**

b. Explain about T-latch with truth table and logic diagram. **(06 Marks)**

Module-4

7 a. Write notes on: i) Noise margin ii) Rise time iii) Fall time in CMOS. **(04 Marks)**

b. Draw and explain realization of CMOS OR gate and AND gate. **(08 Marks)**

c. Explain about NMOS and PMOS with suitable diagram. **(04 Marks)**

OR

8 a. Discuss about CMOS transmission gates and multiplexer. **(08 Marks)**

b. Draw and explain realization of CMOS NOR gate and NAND Gate. **(08 Marks)**

Module-5

9 a. Write a verilog HDL code for SR and D-flipflop. **(10 Marks)**

b. Write a verilog code for up/down counter. **(06 Marks)**

OR

10 a. Write a note on programmable logic array (PLA) and Field Programmable Gate Array (FPGA). **(10 Marks)**

b. Write a verilog HDL code for 4 bit ALU design by behavior model method. **(06 Marks)**

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